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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P7299 Total Pages 3

First Named Inventor or Application Identifier Leslie E. Cline

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ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 24)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 9)

4. X Oath or Declaration (Total Pages 4) Unexecuted)

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. ______ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

a. ____ Computer Readable Copy

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c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ______ Assignment Papers (cover sheet & documents(s))

9. ______ a. 37 CFR 3.73(b) Statement (where there is an assignee)

   __X__ b. Power of Attorney (Unexecuted)

10. ______ English Translation Document (if applicable)

11. ______ a. Information Disclosure Statement (IDS)/PTO-1449

    ______ b. Copies of IDS Citations

12. ______ Preliminary Amendment

13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)

14. ______ a. Small Entity Statement(s)

    ______ b. Statement filed in prior application, Status still proper and desired

15. ______ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. __X__ Other: Attorney signature page including Copy of postcard and Certificate of Express Mailing pursuant to CFR §1.10.

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

____ Continuation ____ Divisional ____ Continuation-in-part (CIP)

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or

__**X**__ Correspondence Address Below

NAME Dennis A. Nicholls, Reg. No. 42,036

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

ADDRESS 12400 Wilshire Boulevard

Seventh Floor

CITY Los Angeles STATE California ZIP CODE 90025-1026

Country U.S.A. TELEPHONE (408) 720-8598 FAX (408) 720-9397

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 31 March, 2000 By _____
Dennis A. Nicholls
Reg. No. 42,036

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8598

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BSTZ File No.: 42390.P7299 Atty/Secty Initials: JPW/DAN/td
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☐ Other: _____

Patent

UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS FOR LOGICAL DETACH FOR A HOT-PLUG-IN DATA BUS

INVENTOR:

LESLIE E. CLINE

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026

(408) 720-8598

ATTORNEY'S DOCKET NO. 42390.P7299

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METHOD AND APPARATUS FOR LOGICAL DETACH FOR A HOT-PLUG-IN DATA BUS

FIELD OF THE INVENTION

The present invention relates to a hot-plug-on data bus, and, more specifically, to a method and apparatus for logically attaching and detaching devices from a hot-plug-in data bus.

BACKGROUND

Many kinds of data buses have been developed for use in computer systems. Most of the early examples required that the computer system be powered down when attaching or detaching a device from the data bus.

More recently, buses have been designed that allow devices to be attached not only when the computer system is powered on, but moreover when the computer system is running. Software may recognize newly attached devices and enable their use without having to reboot the operating system. Buses that operate in this manner may be referred to as hot-plug-in data buses. Common examples of hot-plug-in data buses include the Universal Serial Bus (USB) (Universal Serial Bus Specification Compaq/Intel/Microsoft/NEC Revision 1.1, published September 23, 1998), the Personal Computer Memory Card International Association (PCMCIA) PC Card bus (PCMCIA PC Card Standard Specification Release 2.01, published November 1992), and the Institute of Electrical and Electronic Engineers IEEE-1394 bus (IEEE Standard for

a High Performance Serial Bus, IEEE Std. 1394-1995, published August 30, 1996).

Once a device is attached to a hot-plug-in data bus, conventional operating system software schedules the periodic examination of the device (called "polling") to see if the device wishes to transfer data. However, there are times when it would be advantageous for the computer system to enter into a reduced power state. The computer system operating system may be prevented from allowing the entry into a reduced power state due to the polling schedule. The user would be required to physically detach the device or devices from the computer system in order to permit the entry into the reduced power state. Alternatively, non-standard operating system software could be written. Neither of these two alternatives are desirable.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

Figure 1 is a tree connection diagram of a universal serial bus (USB) system.

Figure 2 is a cable signaling diagram of a USB wire segment.

Figure 3A is a schematic diagram of a pull-up resistor for a USB full-speed mode connection.

Figure 3B is a schematic diagram of a pull-up resistor for a USB low-speed mode connection.

Figure 4 is a state diagram of a logical attach/detach function, according to one embodiment.

Figure 5 is a schematic diagram of a USB logical attach/detach connection, according to one embodiment of the present invention.

Figure 6 is a schematic diagram of a USB logical attach/detach connection, according to another embodiment of the present invention

Figure 7 is a schematic diagram of an IEEE 1394 bus connection.

Figure 8 is a schematic diagram of an IEEE 1394 bus pull-up resistor bias source.

Figure 9 is a schematic diagram of an IEEE 1394 logical attach/detach connection, according to one embodiment of the present invention.

DETAILED DESCRIPTION

A method and apparatus for performing logical attachments and detachments in a hot-plug-in data bus is described. A hot-plug-in data bus may utilize pull-down resistors to keep bus signals near a low voltage level when bus units are physically detached. Active pull-up resistors may then raise the bus signals away from ground when the bus units are physically attached via cabling or other forms of interconnection. The pull-up resistors may be switched away from the pull-up voltage source, which allows the remaining pull-down resistors to pull the bus signals down to the voltage levels corresponding to physical detachment of the cabling.

Referring now to Figure 1, a tree connection diagram of a universal serial bus (USB) system 100 is shown. The USB system 100 includes a multi-segment bus designed to add or remove low and medium speed peripherals to a central USB host 102. The topology of USB system 100 is called a tiered star. Central USB host 102 has an associated root hub 104 which functions as the master attachment point in USB system 100. This is called a root tier 140. Other devices are attached to USB system 100 at differing degrees of remoteness, called tiers. Each tier is numbered by the number of wire segments signals from devices within the tier must pass to reach the root hub 104. For example, hub 1 106 is connected via a single wire segment 160 to root hub 104 in the root tier 140, so hub 1 106 is said to occupy tier 1 142. Similarly, node 120 is attached indirectly to root hub 104 via 3 wire segments 172, 162, 160, so node 120 is said to occupy tier 3 146.

USB devices are either "hubs" for providing additional attachment points or "functions" for providing peripheral devices for USB host 102. Each USB wire segment has two endpoints. One endpoint serves as a hub port attachment and the other endpoint serves as a function attachment. The wire segments of USB system 100 may be physically attached and physically detached during host 102 operations. Each hub in a USB system 100 can detect the physical presence or physical absence of connected lower-tier devices. For example, if wire segment 168 is physically detached, hub 2 108 recognizes the detachment of all lower-tier devices, namely hub 4 116, node 124, and node 126.

Referring now to Figure 2, a cable signaling diagram of a USB wire segment 200 is shown. USB uses 4 signal wires in each wire segment 200. These 4 signal wires are Vbus 202, D+ 204, D- 206, and GND 208. Each end of USB wire segment 200 is normally terminated with a 4 pin connector (not shown).

Vbus 202 carries a nominal +5 Vdc signal, whose source is the upstream (next-highest tier level) hub. Vbus 202 provides a signal that may be used not only as a reference voltage but also as a power supply for low-powered USB devices. Similarly, GND 208 carries a power ground and signal ground signal, whose source is also the upstream hub.

D+ 204 and D- 206 signal wires carry the data signals of the USB wire segment 200 as a differential pair. In most applications, D+ 204 and D- 206 signal wires are implemented as a twisted pair within USB wire segment 200. Two kinds of USB data transfers are supported, referred to as USB full-speed mode and USB low-speed mode. The USB

full-speed mode transfers data at a 12.0 Megabit per second (Mb/s) signaling bit rate. The USB low-speed mode transfers data at a 1.5 Mb/s signaling bit rate. Both modes can be supported in the same USB system by automatic dynamic switching between transfers. A non-return-to zero inverted (NRZI) clock travels down the D+ 204 and D- 206 signal wires along with the data.

Referring now to Figure 3A, a schematic diagram of a pull-up resistor for a USB full-speed mode connection is shown. Hub port 310 is connected to full-speed function 330 via USB wire segment 302. Hub port 310 may in other embodiments be a root hub port. Hub port 310 includes a USB transceiver 312, which supports both full-speed mode and low-speed mode. Prior to USB wire segment 302 being physically connected between hub port 310 and full-speed function 330, pull-down resistors Rpd 314 and Rpd 316 keep the local D- 320 and D+ 318 signal wires, respectively, near reference ground level.

Function 330 includes a full-speed USB transceiver 332 with associated pull-up resistor Rpu 322. Pull-up resistor Rpu 322 is connected on one end to a voltage source, usually a nominal +5 Vdc, and is connected at the other end to the local D+ 318 signal wire. Once USB wire segment 302 is physically connected, pull-up resistor Rpu 322 causes a positive offset on the D+ 318 signal wire with respect to the D- 320 signal wire. This positive offset is interpreted by USB transceiver 312 of hub port 310 as indicating that full-speed function 330 will, in fact, exchange data using the USB full-speed mode.

Referring now to Figure 3B, a schematic diagram of a pull-up resistor for a USB low-speed mode connection is shown. Hub port 340 is

connected to low-speed function 360 via USB wire segment 336. Hub port 340 may in other embodiments be a root hub port. Hub port 340 includes a USB transceiver 342, which supports both full-speed mode and low-speed mode. As explained above in connection with Figure 3A, prior to USB wire segment 336 being connected between hub port 340 and low-speed function 360, pull-down resistors Rpd 344 and Rpd 346 keep the local D- 350 and D+ 348 signal wires, respectively, near reference ground level.

Function 360 includes a low-speed USB transceiver 362 with associated pull-up resistor Rpu 352. Pull-up resistor Rpu 352 is connected on one end to a voltage source, usually a nominal +5 Vdc, and, in contrast with the example of Figure 3A, is connected at the other end to the local D- 350 signal wire. Once USB wire segment 336 is connected, pull-up resistor Rpu 352 causes a positive offset on the D- 350 signal wire with respect to the D+ 348 signal wire. This positive offset is interpreted by USB transceiver 342 of hub port 340 as indicating that low-speed function 360 will, in fact, exchange data using the USB low-speed mode.

In both the Figure 3A and Figure 3B embodiments, a second inference is drawn by hub ports 310, 340. The presence of a positive voltage offset on either the D- 320, 350 signal line or the D+ 318, 348 signal line indicates that a function is physically attached via a USB wire segment 302, 336. This indication may be used by hub ports 310, 340 to indicate up through the various tiers of attachment to the host that the function is physically attached. When the host is made aaware of the physical attachment of the function, host software may continuously poll

the function for data transfers. When the function is quiescent, this polling is unnecessary and may preclude the host from entering into a low-power standby state.

In the Figure 3A and Figure 3B embodiments, the only way to cause the host software to cease unnecessary polling of a quiescent function is to physically detach USB wire segment 302, 336 at one or both ends. This physical detachment requires operator intervention. The need for operator attention and intervention may defeat the purpose of automatic systems for host entry into a low-power state due to lack of system activity.

Referring now to Figure 4, a state diagram of a logical attach/detach function is shown, according to one embodiment. In the Figure 3A and Figure 3B embodiments, a physical detachment was required to prevent unnecessary polling of a quiescent function. The logical attach/detach function described in the Figure 4 embodiment allows a logical detachment as well as a physical detachment to prevent unnecessary polling when the logical detach function is quiescent.

The logical attach/detach function may include 5 operational states. These may include state 0 410, state 1 420, state 3 440, and state 4 450. All of these states presume that the logical attach/detach function is physically attached to a host via a USB wire segment.

In state 0 410, the logical attach/detach function is powered off. When the host computer is powered on, the Vbus signal on the Vbus signal wire within a USB wire segment arrives at the logical attach/detach function, causing a power on transition 460. At this time logical attach/detach function enters state 3 440, which is a normal

standby state. In state 3 440, the logical attach/detach function is logically detached from the host.

While the logical attach/detach function is in state 3 440, the logical attach/detach function may determine that it requires data transmission to or from the host. A wake up signal WAK# assert transition 462 may be caused by the WAK# signal being asserted from the logical attach/detach function to the host. At this time the logical attach/detach function may enter state 4 450, an attention required state. In state 4 450 the logical attach/detach function remains logically detached from the host, but a wake up request is pending. When the host responds to the wake up request, WAK# de-assert transition 464 may be caused by the WAK# signal being de-asserted from the logical attach/detach function to the host. After WAK# de-assert transition 464 the logical attach/detach function re-enters state 3 440.

After responding to a WAK# signal, the host may then perform a logical attach transition 466, which places the logical attach/detach function into state 1 420. In state 1 420, the logical attach/detach function is logically attached to the host, and the host may recognize the attached status of the logical attach/detach function as a full-speed USB device or a low-speed USB device using standard USB protocols. While in state 1 420, and after the host recognizes the attached status of the logical attach/detach function, regular USB data transmissions may occur. When USB data transmissions are no longer required, the host may perform a logical detach transition 468. The logical detach transition 468 places the logical attach/detach function back into state 3

440, causing the logical attach/detach function to again be logically detached from the host.

It is noteworthy that both state 1 420 and state 4 450 may be occupied at the same time by the logical attach/detach function. The logical attach/detach function may cause a WAK# assert transition 462, causing the logical attach/detach function to enter state 4 450. The host may then perform a logical attach transition 466 placing the logical attach/detach function simultaneously into state 1 420. Then, when the logical attach/detach function determines that USB data transfers are no longer required, the logical attach/detach function may then cause a WAK# de-assert transition 464, causing the logical attach/detach function to exit state 4 450 while remaining in state 1 420. Once the host recognizes the WAK# de-assert transition 464, the host may then perform a logical detach transition 468, causing the logical attach/detach function to exit state 1 420 and reenter state 3 440.

Referring now to Figure 5, a schematic diagram of a USB logical attach/detach connection is shown, according to one embodiment of the present invention. In the Figure 5 embodiment, a single high-speed USB logical attach/detach function 540 is connected to the host 510 via an enhanced USB wire segment 530. In other embodiments, a low-speed USB logical attach/detach function may be used, and more than one USB function may be connected to host 510. The Figure 5 embodiment is an exemplary bluetooth on USB module, which allows wireless connection to peripherals (not shown). However, in other embodiments any other functionality may be realized by a logical attach/detach function.

In the Figure 5 embodiment, logical attach/detach function 540 transfers data with host 510 using standard USB signals on D+ signal wire 524 and D- signal wire 526. Baseband signal controller 548 performs the data transfers on the D+ signal wire 524 and D- signal wire 526, and additionally may assert a wake-up signal WAK# on WAK# signal wire 554. Because logical attach/detach function 540 is a full-speed USB function, pull-up resistor 546 is attached at one end to D+ signal wire 524. In other embodiments where logical attach/detach function 540 is a low-speed USB function, pull-up resistor 546 may be attached to the D- signal wire 526 instead. In either case the other end of pull-up resistor 546 is indirectly connected to a biasing voltage through pull-up control 544.

Host 510 includes a power switch 512, a power supply 514, and a host root hub 528. Under logical control of the host 510, power switch 512 may signal the power supply 514 over power supply control signal wire 508. Power supply 514 may then supply power over the Vbus signal wire 518 to logical attach/detach function 540, and may also supply power over the root hub power signal wire 522 to host root hub 528. The following Figure 5 discussion generally presumes that power supply 514 is supplying power over Vbus signal wire 518 and root hub power signal wire 522.

The power switch 512 may additionally consider the logical state of a WAK# signal on WAK# signal wire 554. When logical attach/detach function 540 asserts WAK#, power switch 512 may then assert a host-power (HPWR) signal on HPWR signal wire 516. Logical attach/detach function 540 may assert WAK# when logical attach/detach function 540

is logically detached but begins to receive data. At other times, the power switch 512 may assert HPWR signal on HPWR signal wire 516 in response to requirements of the host 510. An example of the latter would be when the host 510 wished to make a transmission via logical attach/detach function 540.

The HPWR signal is one form of a detach control signal. When a HPWR signal is asserted on HPWR signal wire 516, pull-up control 544 may connect the Vbus signal from Vbus signal wire 518 to the end of pull-up resistor 546 opposite from the D+ signal wire 524. Pull-up resistor 546 then causes a positive offset on the D+ signal wire 524, which may be recognized by host root hub 528 as a logical attachment of logical attach/detach function 540.

Conversely, when baseband signal controller 548 de-asserts WAK# on WAK# signal line 554, power switch 512 may act on this advisory signal by de-asserting the HPWR signal on HPWR signal line 516. In other situations, power switch 510 may de-assert HPWR in response to requirements of host 510, such as when a data transmission is finished. When HPWR signal is de-asserted, pull-up control 544 may then disconnect the Vbus signal from the Vbus signal wire 518 to the end of pull-up resistor 546 opposite from the D+ signal wire 524. Pull-up resistor 546 then no longer causes a positive offset on the D+ signal wire 524. Since the standard USB pull-down resistors 560, 562 act to pull the D+ and D- signals, respectively, towards ground, the host root hub 528 cannot recognize that logical attach/detach function 540 is, in fact, attached. This situation is one form of a logically detached state. Pull-up control 544 has denied a biasing voltage from pull-up resistor 546,

and the resulting lack of offsets on the D+ signal wire 524 and D- signal wire 526 causes a logically detached state. This logically detached state is indistinguishable from a physically detached state from the viewpoint of the host root hub 528.

In the Figure 5 embodiment, pull-up control 544 may be a switch, in some embodiments either a bipolar transistor or a metal-oxide-semiconductor field-effect-transistor (MOSFET). In other embodiments, a junction-field-effect-transistor (JFET) or a mechanical relay may be used, or any other device which may switch power or signals.

Referring now to Figure 6, a schematic diagram of a USB logical attach/detach connection is shown, according to another embodiment of the present invention. In the Figure 6 embodiment, a single high-speed USB logical attach/detach function 640 is connected to the host 610 via an enhanced USB wire segment 630, in a similar manner to the Figure 5 embodiment. In the Figure 6 embodiment, logical attach/detach function 640 transfers data with host 610 using standard USB signals on D+ signal wire 624 and D- signal wire 626. Baseband signal controller 648 performs the data transfers on the D+ signal wire 624 and D- signal wire 626, and additionally may assert a wake up WAK# signal on WAK# signal wire 654. Because logical attach/detach function 640 is a full-speed USB function, pull-up resistor 646 is attached at one end to D+ signal wire 624.

Host 610 includes a power switch 612, a power supply 614, and a host root hub 628. Under logical control of the host 610, power switch 612 may signal the power supply 614 over power supply control signal wire 608. Power supply 614 may then supply power over the Vbus signal

wire 618 to logical attach/detach function 640. The following Figure 6 discussion generally presumes that power supply 614 is supplying power over Vbus signal wire 618.

In contrast to the Figure 5 embodiment, in the Figure 6 embodiment the host root hub 628 may consider the logical state of a WAK# signal on WAK# signal wire 654. When logical attach/detach function 640 asserts WAK#, host root hub 628 may signal the power switch 612 over power switch control signal wire 616. The power switch 612 may then in turn signal the power supply 614 over power supply control signal wire 608. Power supply 614 may then supply a signal HPWR on HPWR signal wire 622 to pull-up control 644 and power regulator 642. In other situations, the power switch 612 may assert HPWR signal on HPWR signal wire 622 in response to requirements of host 610.

When signal HPWR is asserted on HPWR signal wire 622, pull-up control 644 may connect the Vbus signal from Vbus signal wire 618 to the end of pull-up resistor 646 opposite from the D+ signal wire 624. Pull-up resistor 646 then causes a positive offset on the D+ signal wire 624, which may be recognized by host root hub 628 as a logical attachment of logical attach/detach function 640.

Conversely, when baseband signal controller 648 de-asserts WAK# on WAK# signal line 654, host root hub 628 and thence power switch 612 may act on this advisory signal by de-asserting signal HPWR on HPWR signal line 622. In other situations, power switch 612 may de-assert HPWR signal on HPWR signal line 622 in response to requirements from host 610. When signal HPWR is removed, pull-up

control 644 may then disconnect the Vbus signal from the Vbus signal wire 618 to the end of pull-up resistor 646 opposite from the D+ signal wire 624. Pull-up resistor 646 then no longer causes a positive offset on the D+ signal wire 624. Since the standard USB pull-down resistors 660, 662 act to pull the D+ and D- signals, respectively, towards ground, the host root hub 628 cannot recognize that logical attach/detach function 640 is, in fact, attached. This situation is one form of a logically detached state. Pull-up control 644 has denied a biasing voltage from pull-up resistor 646, and the resulting lack of offsets on the D+ signal wire 624 and D- signal wire 626 causes a logically detached state. This logical detached state is indistinguishable from a physically detached state from the viewpoint of the host root hub 628.

Referring now to Figure 7, a schematic diagram of an IEEE 1394 bus connection is shown. In contrast with the USB, the IEEE 1394 bus may connect peers, such as two computers or two intelligent peripherals. Therefore the IEEE 1394 bus is symmetric and provides for physical attachment/detachment recognition for both sides of the interface.

Figure 7 illustrates an IEEE 1394 interface between node Y 710 and node Z 740 via cable segment 730. Cable segment 730 carries signals on two twisted pairs of wires. Each node on the IEEE 1394 interface has circuitry intended for signaling over a twisted pair A and a twisted pair B. For example, for twisted pair A, node Y 710 provides a twisted pair bias source 712, a strobe driver 714, a data receiver 716, a pair of arbitration comparators 718, and a speed receiver 720. For twisted pair B, node Y 710 provides a port status receiver 722, a data driver 724, a strobe receiver 726, and a pair of arbitration comparators

728. In general, the twisted pair A circuits of node Y 710 allow node Y 710 to receive data from the twisted pair B circuits of node Z 740, and the twisted pair B circuits of node Y 710 allow node Y 710 to transmit data to the twisted pair A circuits of node Z 740.

Referring now to Figure 8, a schematic diagram of an IEEE 1394 bus pull-up resistor bias source is shown. Node Z 740 may detect the physical attachment of node Y 710 due to a voltage bias provided by twisted pair bias source 712. Twisted pair bias source 712 includes a pair of pull-up resistors 732, 742, which supply a biasing voltage TpBias to a twisted pair within cable segment 730 when node Z 740 is attached to node Y 710 with cable segment 730. Biasing voltage TpBias is split by the action of the pull-up resistors 732, 734, and the pull-down resistors 736, 738, which are connected at one end to AC ground within node Z 740. Port status receiver 742 may note the presence of this split biasing voltage on the twisted pair wires, and indicate this presence to other circuits within node Z 740 as an indication of the physical attachment of node Y 710.

When node Y 710 is physically detached from node Z 740, the pull-down resistors 736, 738 pull down the voltage on the twisted pair wires. Port status receiver 742 may note the absence of a split biasing voltage on the twisted pair wires, and indicate this absence to other circuits within node Z 740 as an indication of the physical detachment of node Y 710.

It is noteworthy that twisted pair bias source 750 and port status receiver 722 provide a similar capability for node Y 710 to detect the physical attachment and physical detachment of node Z 740.

Referring now to Figure 9, a schematic diagram of an IEEE 1394 logical attach/detach connection is shown, according to one embodiment of the present invention. In the Figure 9 example, node Y 910 may remain physically attached to node Z 940 via cable segment 930. The twisted pair A circuitry of node Y 910 includes a twisted pair bias source 912. The twisted pair bias source 912 includes an amplifier 926, a pair of pull-up resistors 932, 934, a TpBias node 924, and a pull-up control 920. Pull-up control 920 may connect or disconnect biasing voltage TpBias from TpBias node 924 to one end of pull-up resistors 932, 934 under the control of a Y pull-up enable signal on Y pull-up enable signal wire 928. Pull-up control 920 may additionally connect or disconnect biasing voltage TpBias from TpBias node 924 to one end of pull-up resistors 932, 934 under the control of a Z pull-up enable signal on Z pull-up enable signal wire 944.

In a situation where a logical attachment of node Y 910 to node Z 940 is required by node Y 910, called a "local attachment", circuitry within node Y 910 may assert a Y pull-up enable signal on Y pull-up enable signal wire 928. This assertion may cause pull-up control 920 to connect biasing voltage TpBias to one end of pull-up resistors 923, 934. This in turn causes an offset on the twisted pair wires which is detected by port status receiver 942 of node Z 940. The output of port status receiver 942 may be used by other circuitry within node Z 940 to indicate that node Y 910 is logically attached.

Conversely, when a logical attachment of node Y 910 to node Z is required by node Z 940, called a "remote attachment", circuitry within node Z 940 may assert a Z pull-up enable signal on Z pull-up enable

signal wire 944. This assertion again may cause pull-up control 920 to connect biasing voltage TpBias to one end of pull-up resistors 923, 934. This in turn causes an offset on the twisted pair wires which is detected by port status receiver 942 of node Z 940.

When the opposite situation is required, where a logical detachment of node Y 910 to node Z 940 is required by node Y 910, called a "local detachment", circuitry within node Y 910 may de-assert a pull-up enable signal on pull-up enable signal wire 928. This de-assertion may cause pull-up control 920 to disconnect biasing voltage TpBias from one end of pull-up resistors 923, 934. This in turn removes the offset voltage on the twisted pair wires, as the pull-down resistors 936, 938 will pull the twisted pair wires down towards ground. This removal of the offset voltage is detected by port status receiver 942 of node Z 940. The new output of port status receiver 942 may be used by other circuitry within node Z 940 to indicate that node Y 910 is logically detached, even though node Y 910 remains physically attached to node Z 940 via cable segment 930.

Similarly, when a logical detachment of node Y 910 to node Z 940 is required by node Z 940, called a "remote detachment", circuitry within node Z 940 may de-assert a Z pull-up enable signal on Z pull-up enable signal wire 944. This de-assertion may cause pull-up control 920 to disconnect biasing voltage TpBias from one end of pull-up resistors 923, 934. This in turn removes the offset voltage on the twisted pair wires, as the pull-down resistors 936, 938 will pull the twisted pair wires down towards ground. This removal of the offset voltage is again detected by port status receiver 942 of node Z 940.

In the above discussion, a logical detachment detected by port status receiver 942 of node Z 940 could cause node Z 940 to consider itself detached from node Y 910. However, node Y 910 could still detect its own attachment to node Z 940 via twisted pair bias source 950 and port status receiver 922. In the Figure 9 embodiment, this asymmetry exists, and in certain applications may be advantageous. In other embodiments, a pull-up control similar to pull-up control 920 of twisted pair bias source 912 could be configured with twisted pair bias source 950. Each side of the interface could then initiate a logical detachment from or logical attachment to the other side.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method, comprising:

providing a first resistor with a first end and a second end, said first end coupled to a switch and said second end coupled to a data bus wire;

controlling said switch with a detach control signal; and

switching a biasing voltage from said resistor utilizing said switch.

2. The method of claim 1, wherein said first resistor is configured as a pull-down resistor.

3. The method of claim 1, wherein said first resistor is configured as a pull-up resistor.

4. The method of claim 3, further comprising detecting said switching of said biasing voltage.

5. The method of claim 4, further comprising determining a logically detached state responsive to said detecting.

6. The method of claim 1, wherein said detach control signal is responsive to a wake-up signal.

7. The method of claim 6, wherein said detach control signal is asserted when said wake-up signal is de-asserted.

8. An apparatus, comprising:

a first resistor with a first end and a second end;

a switch coupled to said first end of said first resistor and to a bias voltage;

a detach control signal wire coupled to said switch; and

a data bus wire coupled to said second end of said first resistor.

9. The apparatus of claim 8, wherein said switch may apply said bias voltage to said first end of said first resistor responsively to a detach control signal on said detach control signal wire.

10. The apparatus of claim 9, wherein said detach control signal is generated responsively to a wake-up signal.

11. The apparatus of claim 8, wherein said data bus wire carries universal serial bus data.

12. The apparatus of claim 8, wherein said data bus wire carries IEEE-1394 bus data.

13. The apparatus of claim 8, further comprising a second resistor with a first end and a second end, said first end coupled to said data bus wire.

14. The method of claim 13, wherein said second end of said second resistor is coupled to signal ground.

15. An apparatus, comprising:

means for providing a first resistor with a first end and a second end, said first end coupled to a switch and said second end coupled to a data bus wire;

means for controlling said switch with a detach control signal; and

means for switching a biasing voltage from said resistor utilizing said switch.

16. The method of claim 15, wherein said first resistor is configured as a pull-down resistor.

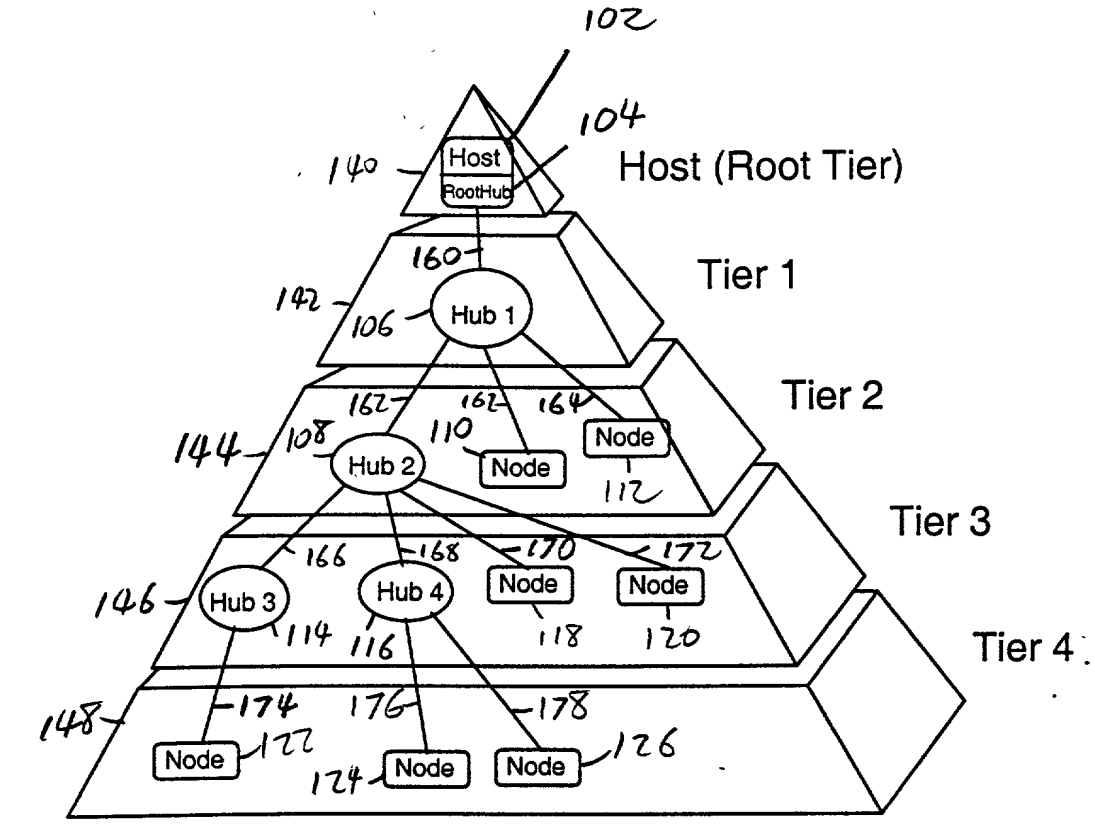
17. The method of claim 15, further comprising

means for detecting said switching of said biasing voltage.

18. The method of claim 15, wherein said detach control signal is responsive to a wake-up signal.

ABSTRACT OF THE DISCLOSURE

A method and apparatus for performing logical attachments and detachments in a hot-plug-in data bus is described. A hot-plug-in data bus may utilize pull-down resistors to keep bus signals near a low voltage level when bus units are physically detached. Active pull-up resistors may then raise the bus signals away from ground when the bus units are physically attached via cabling or other forms of interconnection. The pull-up resistors may be switched away from the pull-up voltage source, which allows the remaining pull-down resistors to pull the bus signals down to the voltage levels corresponding to physical detachment of the cabling.


102
104
140
Host
RootHub
Host (Root Tier)
160
Tier 1
142
106
Hub 1
162
162
164
Tier 2
144
108
110
Hub 2
Node
Node
112
Tier 3
166
168
170
172
146
Hub 3
Hub 4
Node
Node
114
116
118
120
Tier 4
148
174
176
178
Node
122
124
Node
Node
126

100

FIGURE 1

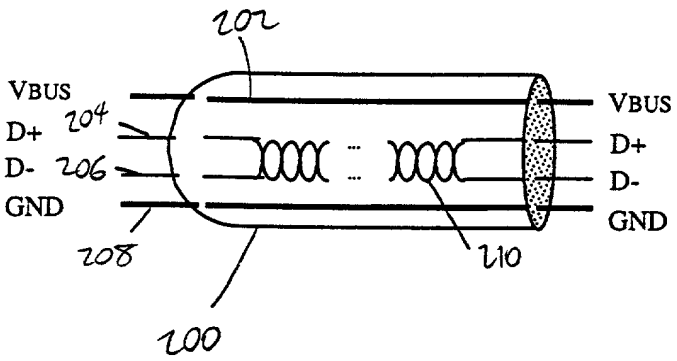
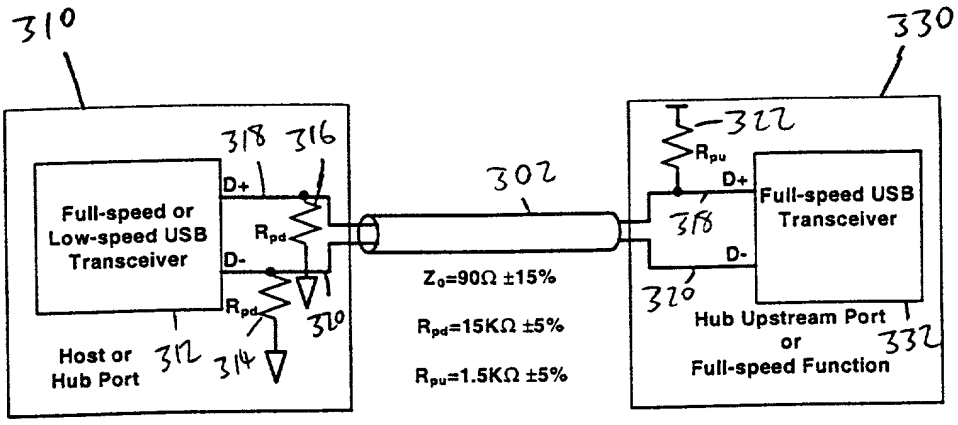
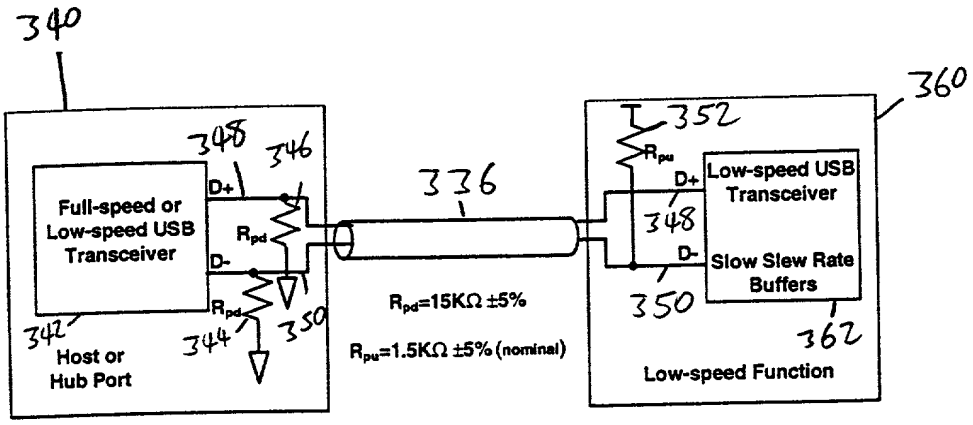


FIGURE 2



Full-speed Device Cable and Resistor Connections

FIGURE 3A



Low-speed Device Cable and Resistor Connections

FIGURE 3B

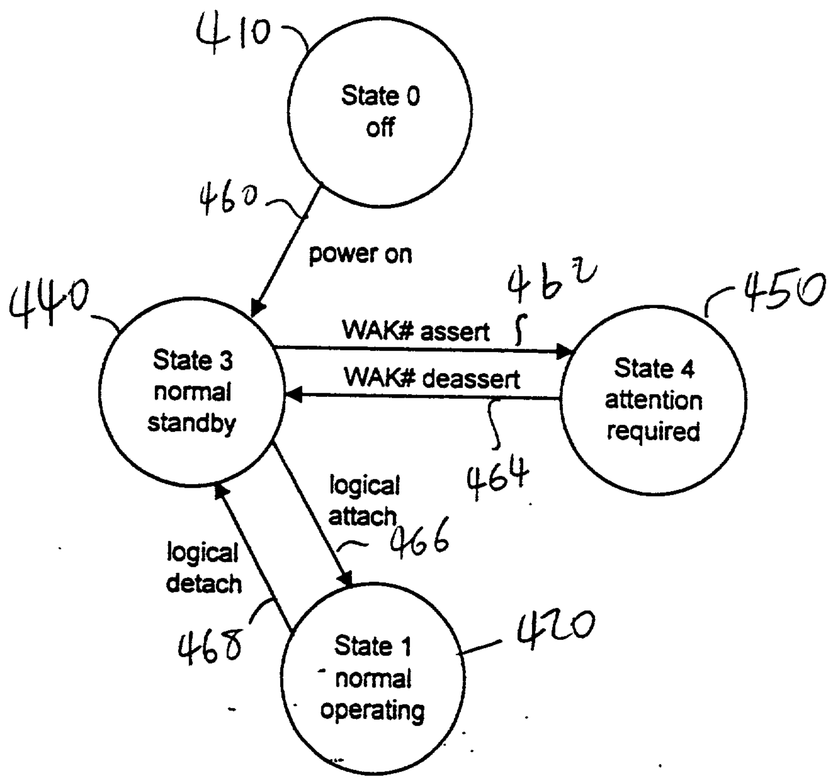

410
State 0
off
460
power on
440
State 3
normal
standby
WAK# assert
462
450
State 4
attention
required
WAK# deassert
464
logical
attach
466
logical
detach
468
State 1
normal
operating
420

FIGURE 4

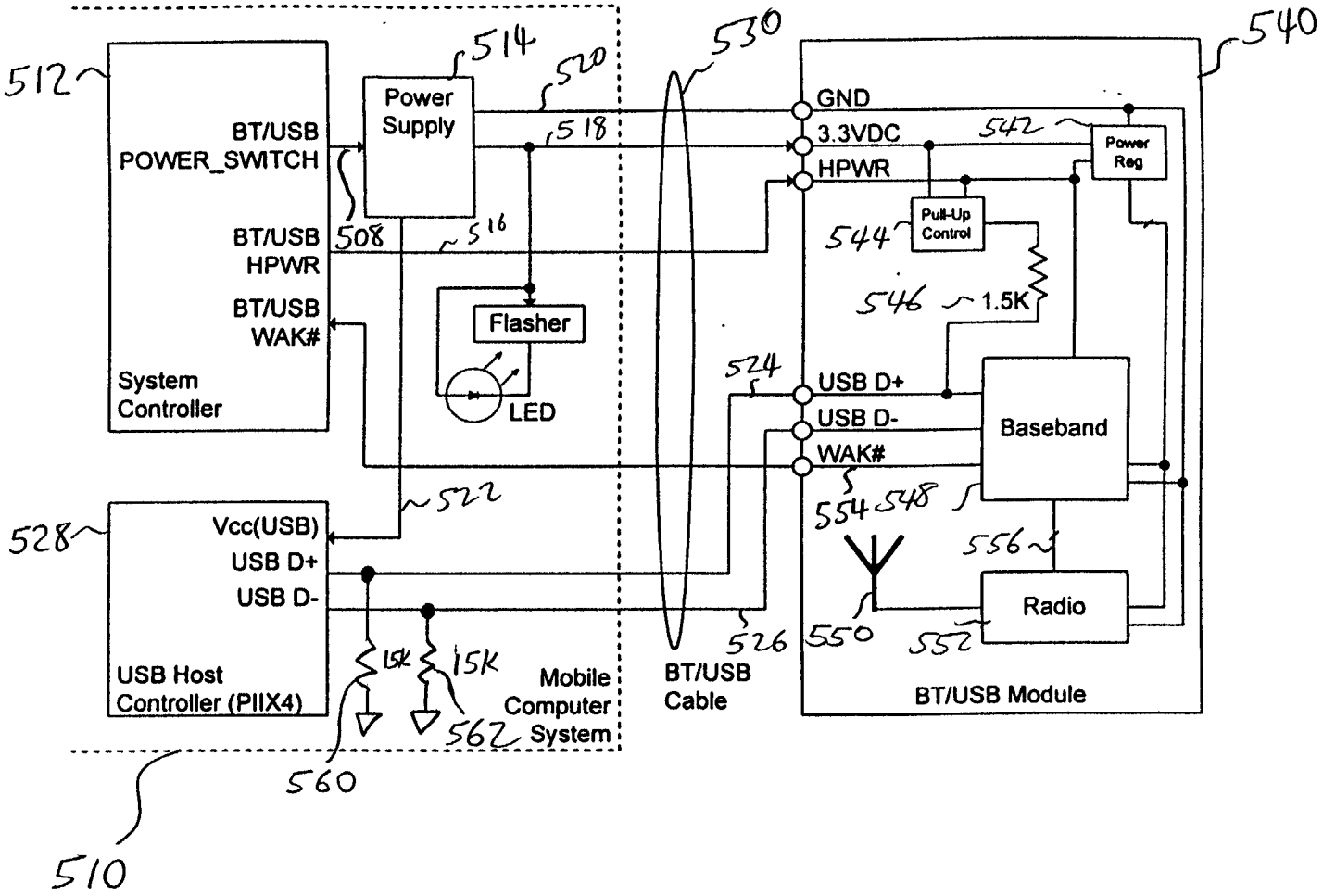

512
514
520
530
540
Power Supply
518
BT/USB POWER_SWITCH
BT/USB HPWR
508
516
BT/USB WAK#
System Controller
Flasher
LED
GND
3.3VDC
HPWR
542
Power Reg
Pull-Up Control
544
546
1.5K
524
USB D+
USB D-
WAK#
Baseband
554
548
556
Radio
550
552
526
522
528
Vcc(USB)
USB D+
USB D-
USB Host Controller (PIIX4)
15K
15K
562
560
Mobile Computer System
BT/USB Cable
BT/USB Module
510

FIGURE 5

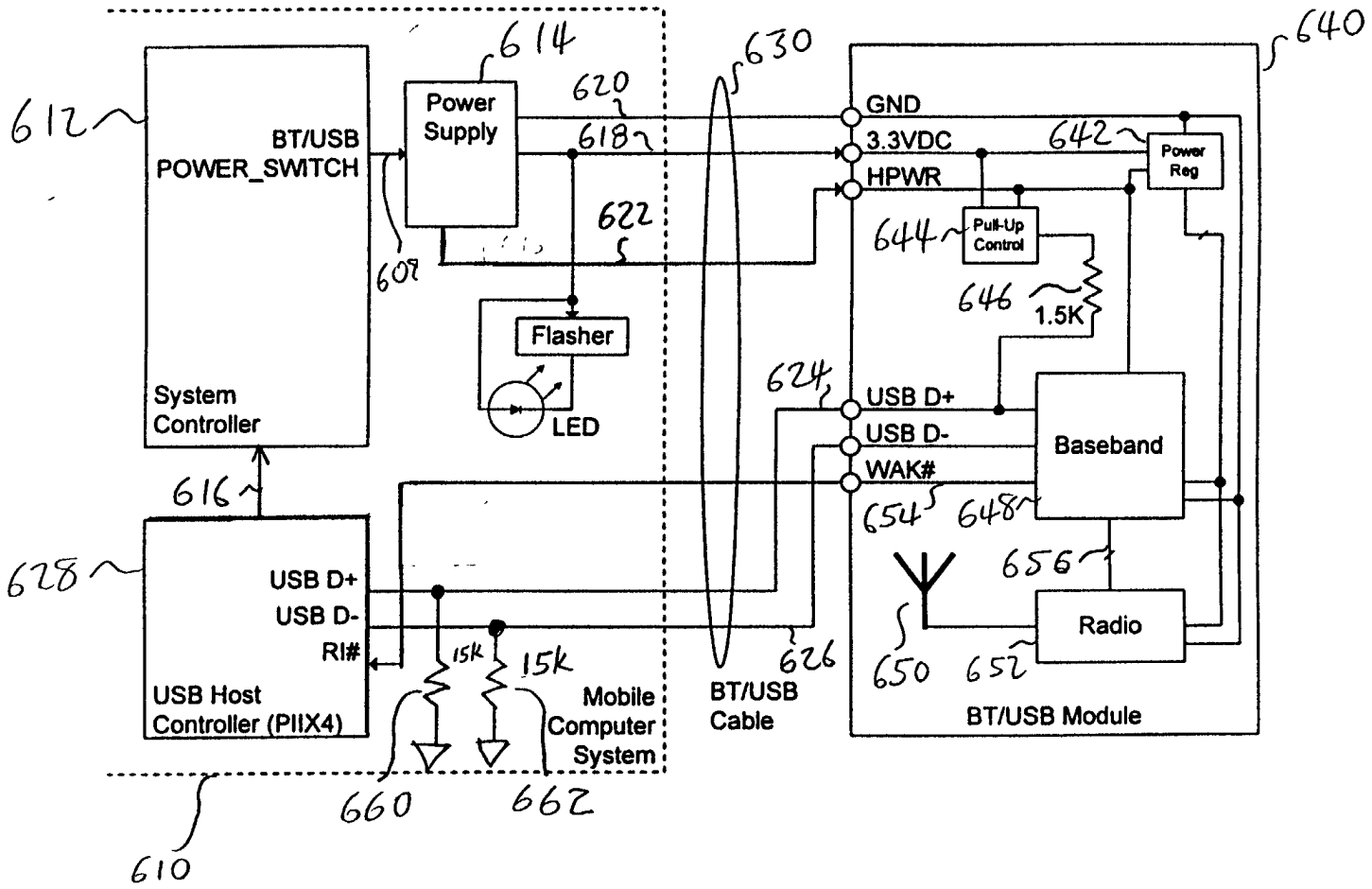


FIGURE 6

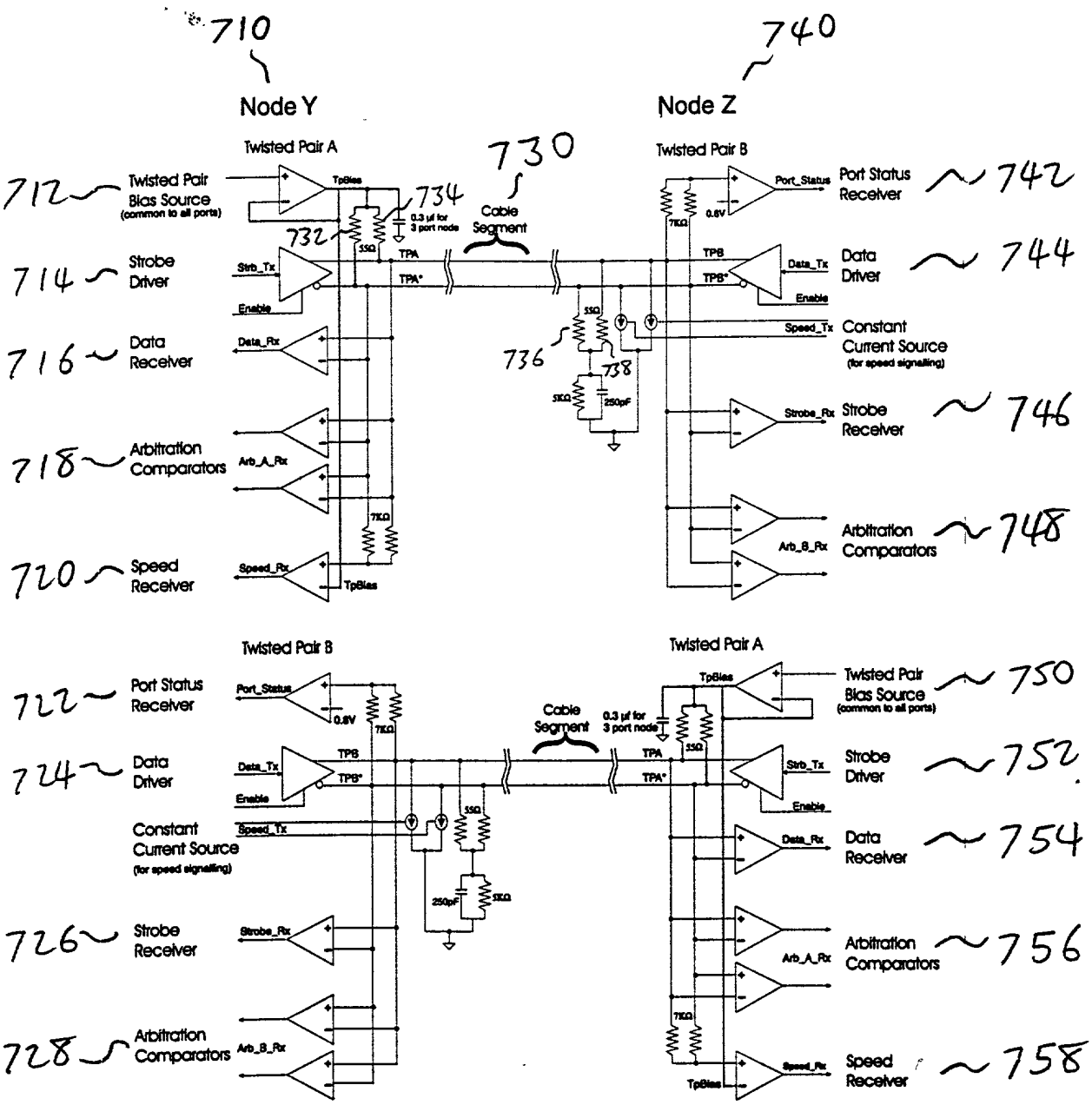
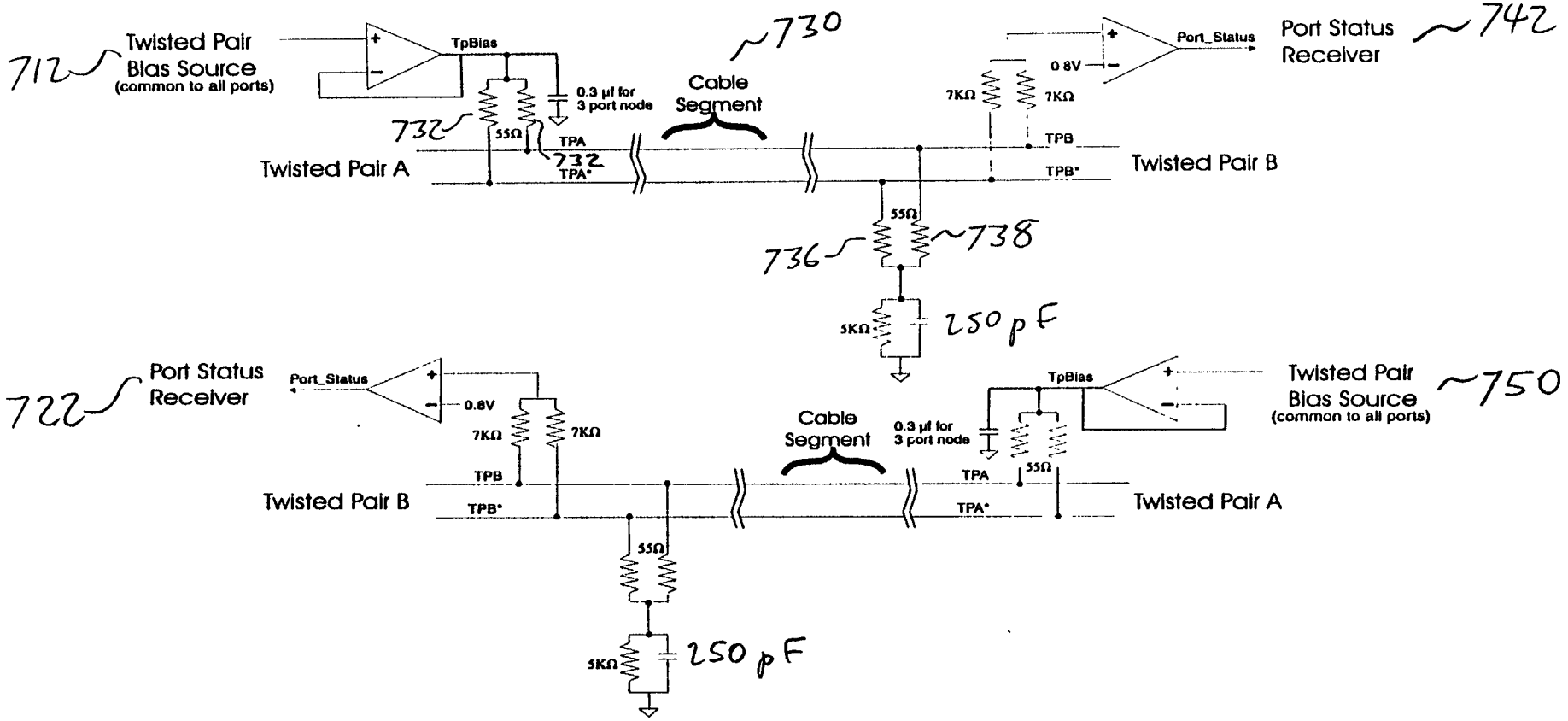

710
Node Y
740
Node Z
Twisted Pair A
Twisted Pair B
730
Cable Segment
712 Twisted Pair Bias Source (common to all ports)
714 Strobe Driver
716 Data Receiver
718 Arbitration Comparators
720 Speed Receiver
732
734
0.3 µf for 3 port node
736
738
742 Port Status Receiver
744 Data Driver
746 Strobe Receiver
748 Arbitration Comparators
Constant Current Source (for speed signalling)
722 Port Status Receiver
724 Data Driver
726 Strobe Receiver
728 Arbitration Comparators
750 Twisted Pair Bias Source (common to all ports)
752 Strobe Driver
754 Data Receiver
756 Arbitration Comparators
758 Speed Receiver
TPA
TPA*
TPB
TPB*
55Ω
7KΩ
5KΩ
250pF
0.8V

FIGURE 7



NODE Y

710

NODE Z

740

FIGURE 8

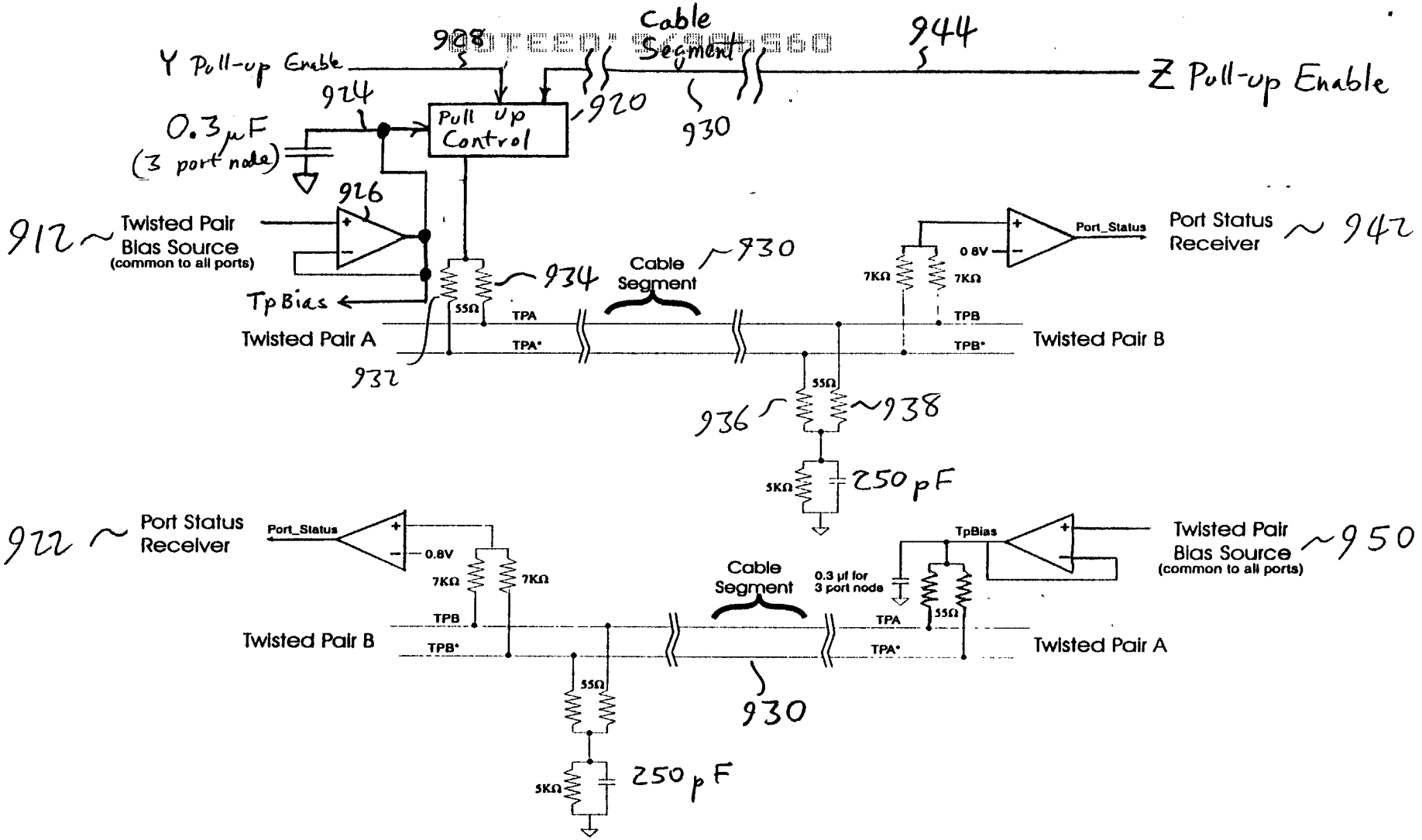

Y Pull-up Enable
928
Cable Segment
944
Z Pull-up Enable
924
0.3 μF
(3 port node)
Pull up Control
920
930
926
912
Twisted Pair Bias Source
(common to all ports)
Tp Bias
934
Cable Segment
930
Port_Status
Port Status Receiver
942
0.8V
7KΩ
7KΩ
TPB
TPB*
Twisted Pair B
Twisted Pair A
TPA
TPA*
55Ω
932
936
938
5KΩ
250 pF
922
Port Status Receiver
Port_Status
0.8V
7KΩ
7KΩ
TPB
TPB*
Twisted Pair B
Cable Segment
930
0.3 μf for 3 port node
TpBias
Twisted Pair Bias Source
(common to all ports)
950
TPA
TPA*
55Ω
Twisted Pair A
55Ω
5KΩ
250 pF
NODE Y
910
NODE Z
940

FIGURE 9

Attorney's Docket No.:42390.P7299 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND APPARATUS FOR LOGICAL DETACH FOR A HOT-PLUG-IN DATA BUS

the specification of which

__X__ is attached hereto.
____ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Dennis A. Nicholls **(Name of Attorney or Agent)**, **BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to** Dennis A. Nicholls **(Name of Attorney or Agent)**, **(408) 720-8300.**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Leslie E. Cline

Inventor's Signature _____ Date _____

Residence Sunnyvale, California (City, State) Citizenship USA (Country)

Post Office Address 649 Madrone Avenue
Sunnyvale, California 94086

APPENDIX A

William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. 44,587; Andrew C. Chen, Reg. No. 43,544; Thomas M. Coester, Reg. No. 39,637; Alin Corie, Reg. No. P46,244; Dennis M. deGuzman, Reg. No. 41,702; Stephen M. De Klerk, under 37 C.F.R. § 10.9(b); Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Sanjeet Dutta, Reg. No. P46,145; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; Paramita Ghosh, Reg. No. 42,806; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Sang Hui Kim, Reg. No. 40,450; Eric T. King, Reg. No. 44,188; Erica W. Kuo, Reg. No. 42,775; Kurt P. Leyendecker, Reg. No. 42,799; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Lisa A. Norris, Reg. No. 44,976; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Daniel E. Ovanezian, Reg. No. 41,236; Marina Portnova, Reg. No. P45,750; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Mark L. Watson, Reg. No. P46,322; Thomas C. Webster, Reg. No. P46,154; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. 45,241; Steven D. Yates, Reg. No. 42,242; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Justin M. Dillon, Reg. No. 42,486; my patent agent, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; John N. Greaves, Reg. No. 40,362; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. 44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.